A novel simultaneous sampling technique and its application to multipoint optical fibre sensor accelerometers

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Abstract – Monitoring large hydroelectric rotating machines requires a multichannel system. Simultaneous sampling of several input channels is needed to avoid the propagation of initial measurement errors. However, this is usually not guaranteed by the acquisition hardware, due to the additional expense involved. The alternative is to correct the error caused by non-simultaneous sampling using digital signal processing techniques. A novel method for real-time, software-based simultaneous sampling using low-order Lagrange interpolation filters is presented. This technique has been implemented in the optoelectronic unit of an optical multipoint accelerometer.

1. Introduction

Monitoring large hydroelectric rotating machines requires measuring multiple signals, which may be divided in two basic groups: very slow time-varying (static) signals (such as temperature or pressure), and dynamic signals with frequency components that may extend into the KHz range (vibration signals). Historically, these analog signals were sent to a control panel, where an operator was in charge of checking the state of every machine in the plant. This process may be automated by capturing those signals with a Digital Acquisition and Signal Processing Unit (DASPU) that processes them and sends the results to a host, where a central data base is established. Thus, the operator may check at any time the state and history of every monitored machine, and data trend and predictive maintenance can be performed.

A system for this purpose has been built, installed and is working in the plant of Villarino (Spain) [1]. The dynamic signals' monitoring system uses six eddy-current displacement sensors from Micro-Epsilon (IS-200-2), altogether with six optical accelerometers developed for this project [2]. The sensors are installed in an orthogonal configuration in the guide bearings of the turbo-generator in three planes along the shaft, Fig. 1.

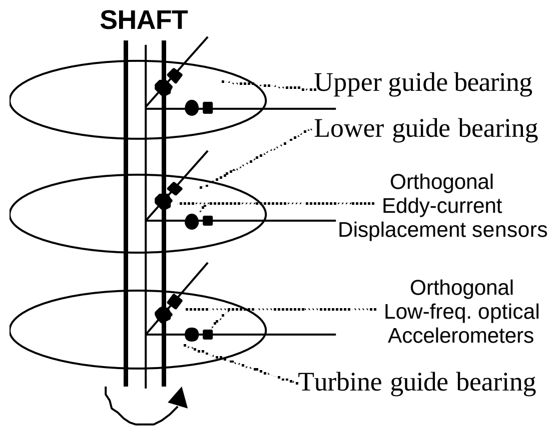

Figure 1. Sensors installation

The optical accelerometers, which are described later, return two optical signals related to the radial bearing's acceleration. These signals are sent to an optoelectronic unit, which processes them and obtains the acceleration. Finally, the resulting acceleration signals, as well as the eddy-current sensors' displacement signals, are sent to the DASPU [3] for further signal processing and storing.

Simultaneous sampling is required in three points along the system's signal processing chain: obtaining the acceleration in the optoelectronic unit, absolute displacement estimation in the DASPU, and orbit composition of the shaft in the three monitored planes. Otherwise any initial error due to non-simultaneous sampling will propagate and may result in severe error. In this paper we focus on the first stage: simultaneous sampling of the two signals received from every sensor in the optoelectronic unit to obtain the acceleration.

However, the acquisition hardware of the optoelectronic unit does not guarantee the simultaneous sampling of the two input signals coming from each accelerometer. Therefore, simultaneous sampling must be achieved afterwards by software through the use of digital signal processing techniques. Two digital signal processing solutions exist: multirate system implementation, and fractional delay filters.

A novel method for real-time simultaneous sampling using simple, low-order fractional delay Lagrange interpolation filters is presented. This technique is computationally efficient and achieves high signal to interpolation noise ratios when the input signals are widely oversampled, which is typical of acquisition systems to simplify the design of the antialiasing filters. Moreover, the interpolation error may be obtained to assure the ADC resolution is maintained.

2. Simultaneous sampling

Simultaneous sampling of all the input channels in a multichannel acquisition system requires a sample&hold for every input channel. However, this is expensive, especially when the number of input channels (N) is high. Thus a multiplexor, followed by a single S&H and ADC is often used. With this configuration a sampling time delay appears between adjacent acquisition channels

$$\Delta T = T_s(MUX) = \frac{T_s}{N} \qquad (1)$$

This delay causes a phase difference between adjacent channels, which means an amplitude error that must be corrected by software to maintain the ADC resolution (B+1 bits). This involves the introduction of a fractional delay of 1/N samples between adjacent channels prior to any signal processing, Fig. 2.

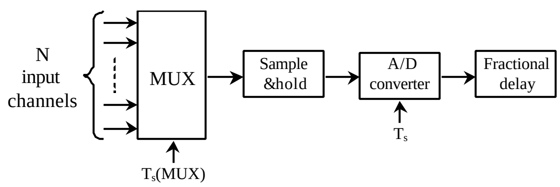

Figure 2. Software simultaneous sampling

A possible solution would be to use a multirate system [4]: interpolate to a sampling rate where the original fractional delay becomes integer, delaying, and decimating back again to the initial sampling rate. This system may be implemented efficiently using a polyphase structure. But, especially when the number of channels that must be simultaneously sampled is high, a more efficient solution computationally exists: using fractional delay filters.

A fractional delay filter is a filter designed for the interpolation between samples of bandwidth-limited signals. Many design methods may be considered [5]: least squared integral error, windowing the ideal reconstruction filter, modelling the filter in frequency with smooth transition band functions, frequency-domain interpolation, etc. Good signal to interpolation noise ratios may be obtained with these methods using medium-order (10-50) filters. But they do not exploit the high oversampling ratio available in most acquisition systems.

An adequate filter design method, when a high oversampling ratio (R) is available, may be found by applying the maximally flat error criterion around $\omega=0$ [6]. That is, given a frequency error which is the difference between the ideal and real filters, the real filter coefficients are obtained by setting the first N+1 derivatives of the error to zero.

$$\left.\frac{\partial^k E\left(e^{jw}\right)}{\partial w^k}\right|_{w=0} = 0 \qquad 0 \le k \le N \tag{2}$$

The coefficients obtained using this design criterion are the same as the ones obtained applying the well-known classical Lagrange interpolation [7]

$$h[n] = \prod_{\substack{i=0 \\ i \neq N-n}}^{N} \frac{N/2 + D - i}{N - n - i} \tag{3}$$

where N/2 is the filter's delay (which already has a fractional part if N is odd) and D the additional fractional delay introduced, which ranges from -0.5 to 0.5. The interpolated signal results:

$$x_i[n] = \sum_{k=0}^{N} x[k]h[n-k] \tag{4}$$

A method for studying the Lagrange filter's error was presented in [8]. To assure the ADC resolution is maintained a worst case error analysis is performed: a tone occupying the full range of the ADC, and maximum input frequency. The fractional delay that causes the highest error is the one that makes the output instants lie exactly between two input samples: D=0.5 for even filter orders, and D=0 for odd ones.

As both the ideal and real filters are LTI systems, the interpolation error is also a tone, whose amplitude may be approximated, generalizing the result of [8], by:

$$A_e = A_o \left(\frac{p}{C_N(D) \cdot R} \right)^{N+1} \tag{5}$$

where A_o is the tone's amplitude, R the oversampling ratio ($R=f_s/2f_o$), and C_N (D) a factor that depends on N and R

$$C_N(D) = \sqrt[N+1]{\frac{(N+1)!}{\prod_{k=0}^{N} \left| \frac{N}{2} + D - k \right|}} \tag{6}$$

To assure the software approach achieves the same resolution as the hardware one, the error's amplitude must be lower or equal to the maximum quantification noise (1/2 LSB). Assuming the full range of the ADC is used, we may obtain two design and analysis equations that relate R, B and N for a bipolar ADC with B+1 resolution bits, or an unipolar ADC with B resolution bits:

$$R \ge \frac{p}{C_N(D)} 2^{(B+1)/(N+1)} \tag{7}$$

$$B + 1 \cong (N+1) \log_2 \frac{R \cdot C_N(D)}{p} \tag{8}$$

In the next table the resolution is shown for several oversampling ratios, and filter orders 0 to 4, in the worst case of fractional delay (D=0 or 0.5).

Table 1. Resolution for different filter orders and oversampling ratios

N	R=2	R=10	R=40
0	0.3	2.7	4.7
1	1.7	6.3	10.3
2	2.0	9.0	15.0
3	2.8	12.1	20.1
4	3.2	14.8	24.8

3. Optoelectronic unit

The acquisition of the bearings' acceleration signals is done using six low-frequency accelerometers, and an optoelectronic unit, implemented originally as a fully analog system [1]. This unit is intended to be replaced by the digital one described here, from which a prototype has been built and is currently working, Fig. 3.

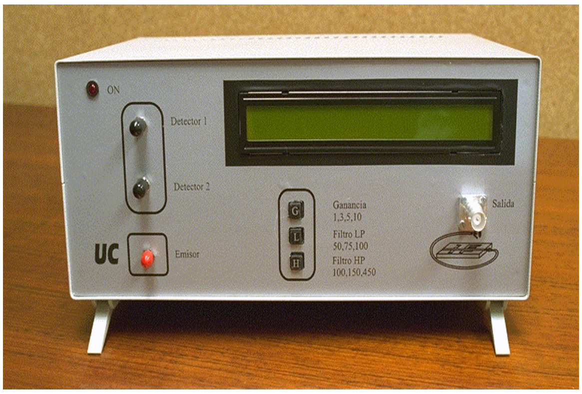

Figure 3. Digital optoelectronic unit

The system's block diagram is shown in fig. 4. The first block of the system is the optical emitter, which is basically a LED excited with a constant current source, and whose optical power is monitored and controlled to compensate the optical system losses. This signal is transmitted using a multimode optical fibre to the sensor's head, which is composed of a single mobile emitting fibre and two fixed ones, fig. 5.

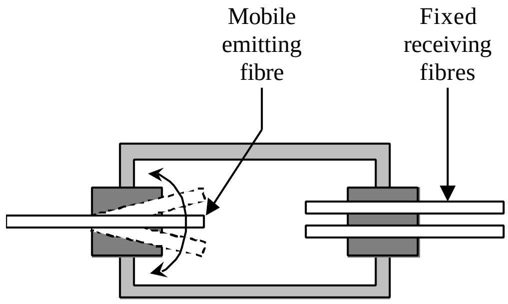

Figure 5. Optical sensors' head

The bearing's orthogonal acceleration to the sensor causes the movement of the emitting fibre and the variation of the light coupled to the two receiving fibres. The detection is done in the optoelectronic unit using a low-noise PIN photodiode, followed by a transimpedance amplifier stage with variable gain (1-2 MV/A).The next block is the acquisition subsystem. This is composed of a cheap 16-channel multiplexor, an analog antialiasing filter based on the MAX274 chip (Butterworth, order 6), and an Analog Interface Circuit which integrates a 14-bit ADC and DAC: TLC32040C.

The last block is based on the TMS320C50 digital signal processor. The acceleration signals are acquired through one of the two serial ports of the C50. The first operation performed by the DSP is to correct the error due to non-simultaneous sampling using a Lagrange interpolation filter. The maximum frequency of interest

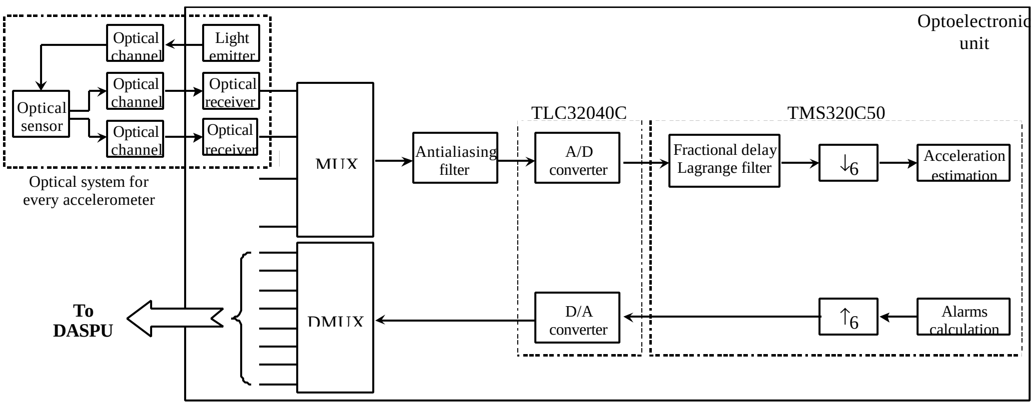

Figure 4. Block diagram of the system

for the input signals is 100 Hz, and the A/D converter's sampling frequency 16 KHz. For 6 optical sensors (12 input channels) this means an oversampling ratio of 6.67 per channel, with a required fractional delay of 0.083 samples between adjacent channels. Using (8) a fourth-order filter is seen to provide 13.93 resolution bits, which are considered enough for this application.

Then a decimation by 6 stage is introduced to work at a rate close to the Nyquist rate, and each sensor's acceleration is calculated using a simple, though non-linear, operation on the two signals:

$$a[n] = K\,\frac{x_2[n] - x_1[n]}{x_2[n] + x_1[n]} \qquad (9)$$

The resulting acceleration signal is interpolated by 6, and sent to the DAC, which works at the same rate as the ADC. These acceleration signals are then demultiplexed, and sent to the DASPU for further signal processing and storing. Additionally, alarms are generated in the optoelectronic unit by comparing the acceleration level with a minimum and a maximum thresholds.

Especial care must be placed in the design of the interpolation and decimation FIR filters, which are designed using the Parks McClellan equiripple method. To keep the 14-bit resolution of the bipolar ADC (10)-(12) are used to obtain the in-band ripple and out of band attenuation. With B+1=14 and $\sigma_x = X_m/\sqrt{2}$ (tone with $A_o=X_m$) this means an in-band ripple of 0.0011 dB, and an out of band attenuation of 85.79 dB, which requires a 45 coefficient FIR filter.

$$r_p \leq 2^{-(B+1)} \qquad (10)$$

$$\mathrm{R}_p(dB) \leq 20 \bullet \log \frac{1 + r_p}{1 - r_p} \qquad (11)$$

$$Attenuation(dB) = 6(B+1) + 4.8 - 20\log\left(\frac{X_m}{s_x}\right) \qquad (12)$$

4. Conclusions

Simultaneous sampling of multiple input channels is a necessity in rotating turbo-generators monitoring. Typically, the data acquisition system uses a high oversampling ratio. This can be exploited to replace the costly hardware scheme by a novel method based in low-order Lagrange interpolation. Through a theoretical study, the error of the Lagrange interpolator can be bounded to keep the ADC resolution. This technique has been used in the opto-electronic unit of a low-frequency multi-channel optical accelerometer, where simultaneous sampling is required between every pair of input channels. A prototype of this unit, based on a TMS320C50 DSP, has been built, tested and is working properly.

References

[1] F. Arregui *et al.* "Protection and Monitoring system for hydroelectric generating sets", *EUROMAINTENANCE*, pp. 741-750, Copenhagen, 1996.

[2] J.M. López-Higuera et al. "Simple low-frequency optical fiber accelerometer with large rotating machine monitoring applications", *Journal of lightwave technology*, vol. 15, no. 7, pp. 1120-1130, July 1997.

[3] J. Ibáñez, M. Lázaro, D. Luengo, I. Santamaría, C. Pantaleón, "Specific DSP based monitoring system for hydro-generator sets", *ICSPAT 1998.*

[4] R.E. Crochiere, L.R. Rabiner, *Multirate digital signal processing*, Ed. Prentice-Hall, N.J., 1983.

[5] T.I. Laakso et al., "Splitting the unit delay: tools for fractional filter design", *IEEE Signal Processing Magazine*, pp. 30-60, January 1996.

[6] C.C. Ko, Y.C. Lim, "Approximation of a variable-length delay line by using tapped delay line processing", *Signal Processing*, no. 14, , pp. 363-369 1988.

[7] P.J. Kootsookos, R.C. Williamson, "FIR approximation of fractional sample delay systems", *IEEE Trans. On Circuits and Systems II,* vol. 43, no. 3, pp. 269-271, March 1996.

[8] D. Luengo, C. Pantaleón, I. Santamaría, J. Ibáñez, "Simultaneous sampling by digital phase correction", *IMTC*, pp. 980-984,19-21 May, 1997.