

## Simultaneous Sampling by Digital Phase Correction

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**Abstract** - Phase correction by digital filtering is a common approach to achieve simultaneous sampling with no additional hardware. In this paper we obtain a bound for the interpolation error as a function of the oversampling ratio of the input signal and the interpolation filter order. This bound can be used to analyze and design simultaneous sampling systems by digital phase correction. The obtained theoretical results are validated through simulation. Finally, a vibration analysis system using this technique is described.

### I. INTRODUCTION

Multichannel acquisition systems often require simultaneous sampling of their input channels. To achieve this, a hardware approach would require using a S/H for each channel, a multiplexer and an A/D [1], Fig. 1.

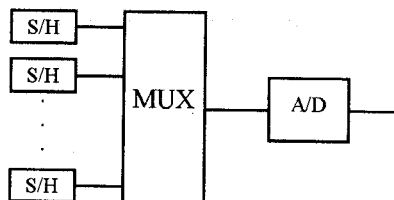


Fig. 1. Hardware approach to simultaneous sampling

The alternative proposed in this paper uses a non-simultaneous sampling scheme followed by a low order interpolation filter. This scheme performs phase compensation after the A/D to achieve simultaneous sampling, Fig. 2.

The obvious advantages of this approach are its minimum hardware requirement (a single S/H for any number of input channels), easy scalability (no new elements for new channels), and reduced size of the PCB.

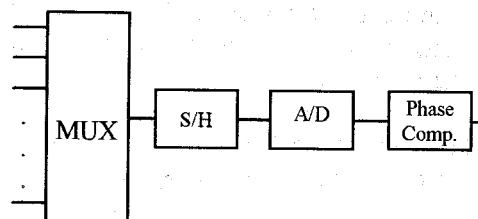


Fig. 2. Simultaneous sampling using software compensation

This approach is not new, [2], [3], [4]. In fact, a fairly wide bibliography is devoted to the design of filters for phase compensation (usually called fractional delay filters), [5], [6], [7]. Although in most practical applications linear interpolation is used.

The main problem of this approach is that the distortion introduced by the phase correction stage is difficult to evaluate. In fact, there is not a general rule for the design of these systems when the resolution of the A/D must be maintained.

In this paper we analyze a simple approach to phase correction based on low order interpolation of oversampled analog signals. The worst error case is considered, which allows us to obtain analysis equations (number of significant bits as a function of oversampling ratio and interpolation order) and design equations (minimum oversampling ratio to achieve a certain resolution).

This approach is possible since signals acquired from many Data Acquisition (DAQ) boards are already highly oversampled to simplify analog antialiasing filters. By increasing the oversampling ratio, the distortion introduced by the phase compensation stage can be made as low as desired.

The theoretical results developed in the paper are validated through simulation. The proposed approach is

implemented in a DSP based vibration analysis system whose performance meets the theoretical bounds.

## II. PHASE COMPENSATION STAGE

### A. Problem Statement

The ideal filter that allows fractional delay with no distortion is given by

$$h_i[n] = \frac{\sin(\pi[n-D])}{\pi[n-D]} \quad (1)$$

Where D is the normalised fractional delay comprised in the range from 0 to 1, measured from sample (N-1)/2 (Nth-order filter delay).

Lagrange interpolation [8] can be implemented as a digital filter, whose impulsive response

$$h[n] = \prod_{\substack{i=0 \\ i \neq N-k}}^N \frac{N-1+2D-2i}{2(N-n-i)} \quad (2)$$

For a zero-order hold,  $h[n]=\delta[n]$ , and for a linear interpolator  $h[n] = D\delta[n]+(1-D)\delta[n-1]$ . The distortion introduced can be evaluated as the difference between (1) and (2).

$$e[n] = x[n] * (h_i[n] - h[n]) = x_{real} - x_{int} \quad (3)$$

The phase compensation error will depend on both the input signal and the normalised fractional delay. Performing a worst case analysis it is possible to obtain a design equation ensuring a given resolution.

The worst case will obviously be a tone varying at the maximum input frequency. For an even-order filter the maximum error appears when  $D=0$  or  $D=1$  and for an odd one when  $D=0.5$ .

Therefore, considering a sinusoidal input of frequency  $f_0$  and substituting (1) y (2) in (3) we have

$$e[n] = A \left\{ \cos \left( \left[ n - \frac{N+1}{2} + D \right] W_R \right) - \sum_{k=0}^N h[k] \cos([n-k] W_R) \right\} \quad (4)$$

Where  $W_R = \pi/R$ , and R is the oversampling ratio,  $R=f_s/2f_0$ . It is straightforward to show that (5) can be written as

$$e[n] = A_e \cos(n W_R + \phi_e) \quad (5)$$

where

$$A_e = A \sqrt{k_1^2 + k_2^2} \quad (6)$$

$$\phi_e = \tan^{-1} \left( \frac{k_2}{k_1} \right) \quad (7)$$

and

$$k_1 = \cos \left( \left[ \frac{N+1}{2} - D \right] W_R \right) - \sum_{k=0}^N h[k] \cos(k W_R) \quad (8)$$

$$k_2 = \sin \left( \left[ \frac{N+1}{2} - D \right] W_R \right) - \sum_{k=0}^N h[k] \sin(k W_R) \quad (9)$$

These are the distortion constants that provide the final precision of the system.

### B. Design and Analysis Equations.

The distortion introduced by the phase correction stage must be lower or equal than half the quantization interval in order to have the same error as real (hardware) simultaneous sampling

$$e[n] < \frac{1}{2} LSB = \frac{X_m}{2^{B+1}} \quad (10)$$

Where the LSB (Least Significant Bit) depends on  $X_m$ , the positive range of the A/D (bipolar), and B+1, number of bits (resolution) of the ADC. If we look for the number of significant bits for a given maximum error ( $e[n]=A_e$ )

$$B = \log_2(X_m) - [1 + \log_2(A_e)] \quad (11)$$

The oversampling ratio required for a given number of significant bits must be obtained in a case by case basis by expanding (8) and (9) in Taylor series and taking the first significant term. In this case one of the distortion constants predominates ( $k_1$  for odd interpolation orders and  $k_2$  for even). Moreover, if the signal uses the full range of the A/D ( $X_m=A$ ), then the following general analysis equation results

$$R \geq \frac{\pi}{C_N} 2^{(B+1)/(N+1)} \quad (12)$$

$$B = (N+1) \log_2 \left( \frac{RC_N}{\pi} \right) - 1 \quad (13)$$

Where  $B+1$  is the number of significant bits,  $k_i$  is the dominant error constant,  $R$  the oversampling ratio, and  $C_N$  a constant that depends solely on the interpolation order.

For example, for the zero-order hold the design and analysis equations reduce to

$$R \geq \frac{\pi}{2} 2^{B+1} \quad (14)$$

$$B = \log_2 \left( \frac{2R}{\pi} \right) - 1 \quad (15)$$

while for a linear interpolator we obtain

$$R \geq \frac{\pi}{\sqrt{8}} 2^{(B+1)/2} \quad (16)$$

$$B = 2 \log_2 \left( \frac{R\sqrt{8}}{\pi} \right) - 1 \quad (17)$$

### III. SIMULATION RESULTS

In this section the results obtained in section II are validated through simulation. The system shown in Fig. 3 has been used to measure the difference between an ideally delayed tone and the interpolated one.

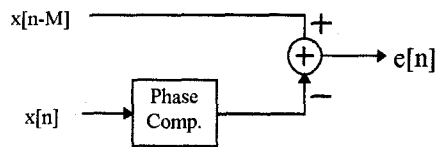


Fig. 3. System used for interpolation error simulation

In Fig. 3  $M$  takes into account the delay of the phase correction filter as well as the fractional delay

$$M = \frac{N+1}{2} - D \quad (18)$$

The simulation has been done with a tone of  $f_m=80$  Hz, for oversampling ratios in the range of 2 to 1024. A delayed tone is generated and compared with the original one (zero phase) that has been compensated.

Once the error  $e[n]$  is obtained in this way the Signal to Noise Ratio (SNR) may be evaluated for different oversampling ratios and interpolation orders. And from the SNR it is immediate to extract the significant bits, Fig. 4.

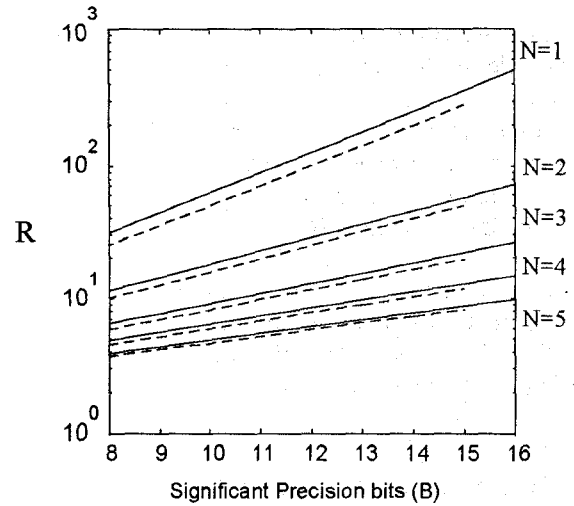


Fig. 4. Significant precision bits (theoretical and estimated) as a function of the oversampling ratio and interpolation order

In Fig. 4 the continuous lines represent the values obtained through simulation and the dotted ones the values calculated theoretically. The difference is seen to be minimum and decrease as the interpolation order increases.

The main conclusion that may be obtained from Fig. 4 is that the greatest decrease in oversampling ratio appears passing from a zero-order interpolator to a linear one. Thus, except for very low oversampling ratios or high precision requirements linear interpolation will be enough in most cases.

From Fig. 4 the constants  $C_N$  are obtained and compared to those calculated theoretically in Table 1. The estimated constants are obtained as the mean of the constants for each value of  $B$  in the simulation. The error committed is due to the deviation that occurs when  $B$  is low and low oversampling ratios are thus required.

Interpolation Order	Theoretical constants	Estimated constants
0	2.00	2.01
1	2.83	2.84
2	2.52	2.54
3	2.56	2.57
4	2.43	2.45
5	2.43	2.38

Table 1. Precision constants for different interpolation orders

#### IV. VIBRATION ANALYSIS SYSTEM USING DIGITAL PHASE CORRECTION

##### A. General description of the system.

The system designed is a monitoring system for hydroelectric machines rotating at speeds from 60 rpm up to 600 rpm. The goal is to measure displacement and acceleration signals of several hydro T-G sets and to correlate them with other parameters that cause distortion. This will allow detection and prevention of possible malfunctioning in the machines.

In this system simultaneous sampling is essential, as one of its final goals is to plot the orbits of the vibration of the shaft in three planes. Non-simultaneous sampling would cause an error that will falsify these orbits.

The basic unit developed for that task will be called DASPU (Data Acquisition & Signal Processing Unit). Static and dynamic variables are measured, so two types of DASPU's are required.

In this section we focus on the Dynamic DASPU. The general diagram of the DASPU components is composed of an Acquisition Unit and a Signal Processing Unit, Fig. 5.

The Acquisition Unit deals with signal conditioning and analog to digital conversion. In this case, conditioning the signals from the sensors involves only analog antialiasing filtering and multiplexing.

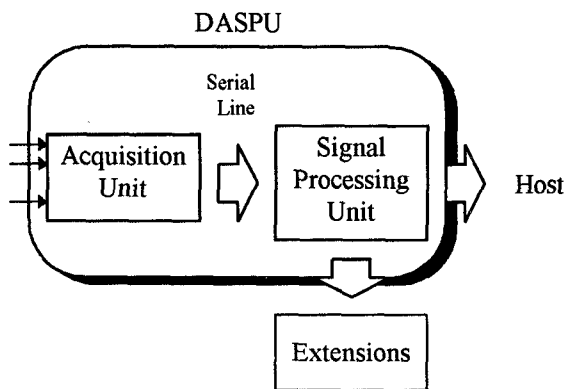


Fig. 5. General vision of DASPU components

The Signal Processing Unit is based on the TMS320C30 Digital Signal Processor (DSP) chip. For practical considerations the signal processing chain is divided in two stages.

Fig. 6 shows The first one which includes phase correction, filtering and a decimation stage to reduce the

high oversampling ratio that is no longer required. This processing is performed on-line

The second part of the signal processing will be done off-line. In this part the displacement and acceleration levels and frequencies of the shaft are obtained, and the orbits of the three planes estimated.

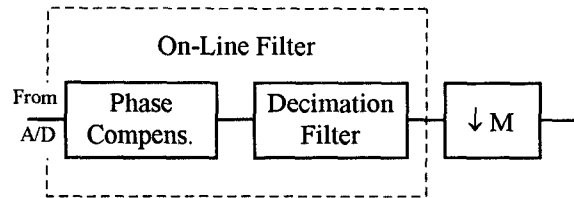


Fig. 6. On-Line Signal Processing

In Table 2 the main characteristics of the system that have an influence in the digital phase correction are shown, while Table 3 shows the Signal to Noise Ratio and resolution obtained for different interpolation orders.

Linear interpolation is used in the system, since it is enough to ensure the precision required. A third order interpolator is not used because it means introducing an additional complexity for almost no gain (the significant bits are limited by the ADC). Practical measures confirm the expected SNR.

A/D Resolution	12 bits
Bandwidth	80 Hz
Sampling Frequency	15625 Hz
Oversampling Ratio	97.65

Table 2. Signal Processing characteristics of the Dynamic DASPU

	SNR (dB)	Resolution (B+1)
0	37.66	5.96 bits
1	73.56	11.92 bits
2	115.43	18.87 bits

Table 3. Resolution and Signal to Noise Ratio considering several interpolation filters

#### IV. CONCLUSIONS

Simultaneous sampling of several input channels can be achieved by digital phase correction filtering. The performance of this approach depends on the oversampling ratio of the input signal and the interpolation order.

In this paper we have developed a bound for the interpolation error of low order Lagrange interpolation

filters. Based on this error, we obtain expressions that relate number of significant bits with oversampling ratio and filter order. The presented theoretical results are validated through simulation: the estimated interpolation errors closely resemble the expected ones. Finally, a vibration analysis system demanding simultaneous sampling is introduced, and the phase correction step designed using the proposed approach.

Other applications of this methodology can be considered: synchronous to a asynchronous conversion, irrational sampling rate conversion, timing adjustment and synchronisation in digital modems, high-resolution pitch prediction,...

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